What is claimed is:

1. A method of manufacturing a photomask, comprising the steps of:

(a) preparing a plurality of first photomasks including one or more resist masks; and

(b) transferring each pattern of said plurality of first photomasks onto a second photomask by reduced projection exposure.

2. The method of manufacturing a photomask according to claim 1, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said second photomask.

3. The method of manufacturing a photomask according to claim 1, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an integrated circuit pattern region of said second photomask.

4. The method of manufacturing a photomask according to claim 1, wherein both of a metal pattern having a light-shielding property to exposure light and an organic film pattern having a light-shielding property or a light-reducing property to exposure light are arranged in an integrated circuit pattern region of said second photomask.

5. The method of manufacturing a photomask according to claim 4, further comprising the step of removing said organic film pattern of said second photomask.

6. A method of manufacturing a photomask, comprising the steps of:

(a) preparing a set of IP masks, at least one of which is made of a resist mask; and

(b) transferring each pattern of said plurality of IP masks onto a product mask by reduced projection exposure.

7. The method of manufacturing a photomask according to claim 6, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

8. The method of manufacturing a photomask according to claim 6, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an integrated circuit pattern region of said product mask.

9. The method of manufacturing a photomask according to claim 6, wherein both of a metal pattern having a light-shielding property to exposure light and an organic film pattern having a light-shielding property or a light-reducing property to exposure light are arranged in an integrated circuit pattern region of said product mask.

10. The method of manufacturing a photomask according to claim 9, further comprising the step of removing said organic film pattern of said product mask.

11. A method of manufacturing a photomask, comprising the steps of:

(a) preparing an IP mask made of a resist mask, which is a photomask used in transfer of a memory mat or an aggregate of the memory mats; and

(b) transferring a pattern of said IP mask onto a product

mask by reduced projection exposure.

12. The method of manufacturing a photomask according to claim 11, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

13. The method of manufacturing a photomask according to claim 11, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an integrated circuit pattern region of said product mask.

14. A method of manufacturing a photomask, comprising the steps of:

(a) preparing a first IP mask made of a resist mask, which is a photomask used in transfer of a memory mat or an aggregate of the memory mats;

(b) preparing a second IP mask made of a resist mask, which is a photomask used in transfer of a peripheral circuit region of said memory mat; and

(c) transferring patterns of said first and second IP masks onto a product mask by reduced projection exposure.

15. The method of manufacturing a photomask according to claim 14, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

16. The method of manufacturing a photomask according to claim 14, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an integrated circuit pattern region of

said product mask.

17. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a set of first photomasks including one or more resist masks;

(b) transferring each pattern of said plurality of first photomasks onto a second photomask by reduced projection exposure; and

(c) transferring the pattern on said second photomask onto a semiconductor wafer by reduced projection exposure.

18. The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said second photomask.

19. The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in the integrated circuit pattern region of said second photomask.

20. The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein both of a metal pattern having a light-shielding property to exposure light and an organic film pattern having a light-shielding property or a light-reducing property to exposure light are arranged in an integrated circuit pattern region of said second photomask.

21. The method of manufacturing a semiconductor

integrated circuit device according to claim 20, further comprising the step of removing said organic film pattern of said second photomask.

22. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a plurality of IP masks, at least one of which is made of a resist mask,

(b) transferring each pattern of said plurality of IP masks onto a product mask by reduced projection exposure;

(c) transferring a pattern of said product mask onto a semiconductor wafer by reduced projection exposure.

23. The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

24. The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an light-shielding pattern of the integrated circuit pattern region of said product mask.

25. The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein both of a metal pattern having a light-shielding property to exposure light and an organic film pattern having a light-shielding property or a light-reducing property to exposure light are arranged in an integrated circuit pattern region of

said product mask.

26. The method of manufacturing a semiconductor integrated circuit device according to claim 25, further comprising the step of removing said organic film pattern of said product mask.

27. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing an IP mask made of a resist mask, which is a photomask used in transfer of a memory mat or an aggregate of the memory mats;

(b) transferring the pattern of said IP mask onto a product mask by reduced projection exposure; and

(c) transferring the pattern of said product mask onto a semiconductor wafer by the reduced projection exposure.

28. The method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

29. The method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an integrated circuit pattern region of said product mask.

30. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a first IP mask made of a resist mask, which is a photomask used in an transfer of a memory mat or an

aggregate of the memory mats;

(b) preparing a second IP mask made of a resist mask, which is a photomask used in an transfer of a peripheral circuit region of said memory mat;

(c) transferring the patterns of said first and second IP masks onto a product mask by reduced projection exposure; and

(d) transferring the pattern of said product mask onto a semiconductor wafer by reduced projection exposure.

31. The method of manufacturing a semiconductor integrated circuit device according to claim 30, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product photomask.

32. The method of manufacturing a semiconductor integrated circuit device according to claim 30, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in the integrated circuit pattern region of said product mask.